MONOLITHICALLY-INTEGRATED NEW DUAL SURGE PROTECTIVE DEVICE AND ITS FABRICATION METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No. 201110003046.5, filed on Jan. 7, 2011, the disclosure of which is herein incorporated herein by reference.

FIELD OF THE INVENTION

[0002] This field relates to a type of surge protective device, more specifically, a type of monolithically-integrated dual surge protective device and its fabrication method

BACKGROUND OF THE INVENTION

[0003] In electronic equipment and systems, there is always some voltage leap, even external interruption, such as static electricity, etc. These types of transient over-voltage are referred as "surge" in general which will affect reliability of the electronic devices and systems. There are many (transient voltage suppressor) TVS devices in the markets, which are used to eliminate the abrupt transient over-voltage.

[0004] In the general knowledge available to persons of ordinary skill, the TVS element is generally an N^+P^+ zener diode or ceramic voltage-variable resistor and adopts the principle of current division that before the protected device or system breaks down, the protector breaks down to guide the current out for the purpose of protecting the subsequent sections. The several TVS devices so far are diode type TVS device, gas discharge tube, crystal tube TVS device, filter, etc.

[0005] There are at least the following defects existing in many conventionally known surge protectors: for example, a device having a single structure and split pattern can only prevent surges of a single form. In practical use, multiple surge protectors on series basis are often adopted to protect system safety so as to meet system demand. Moreover, many conventional surge protectors cannot be integrated within system chips. There remains a need for improved surge protectors.

SUMMARY OF THE INVENTION

[0006] In one preferred example, a monolithically-integrated dual surge protective device, comprises a LDMOS device, and a diode assembly which comprises multiple diodes series-wound on back-to-back basis in the following sequence:

[0007] -N-P- . . . -N-P-N-P-N- . . . -P-N-; wherein one end of the diode assembly is connected to a drain electrode of the LDMOS device and the other end is connected to a gate electrode of the LDMOS device.

[0008] In one preferred embodiment, a method of fabricating the monolithically-integrated dual surge protective device includes the steps of depositing a polysilicon layer having a thickness of 0.5 to 3 microns on a gate oxide layer of the LDMOS device using chemical vapor deposition and mixing a P-type dopant, such as boron, to form P-type polysilicon during the deposition; using photo-etching to define an N-type regions on the polysilicon and using ion injection to inject an N-type dopant, such as phosphorous ions, to form N-type regions in a section; depositing a passivation layer above said polysilicon layer; and connecting a first end of the diode directly to the gate electrode and a second end of drain electrode of the LDMOS device during a process of metallization.

BRIEF DESCRIPTION OF THE FIGURES

[0009] Further features and advantages of the invention will become apparent when the following detailed description is read in view of the drawing figures, in which:

[0010] FIG. **1** shows an equivalent circuit diagram of an exemplary monolithically-integrated dual surge protective device;

[0011] FIG. **2** shows an exemplary cross-sectional view of a diode;

[0012] FIG. **3** shows a structure schematic of a basic profile of an exemplary LDMOS device;

[0013] FIG. **4** shows a structure schematic of the profile of an exemplary monolithically-integrated dual surge protective device;

[0014] FIG. **5** shows a curve of current variation along with the voltage rising at a drain electrode of an exemplary monolithically-integrated dual surge protective device along with voltage rising at the drain electrode.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The examples and drawings provided in the detailed description are merely examples, which should not be used to limit the scope of the claims in any claim construction or interpretation.

[0016] The term LDMOS" is an abbreviation for laterally diffused metal oxide semiconductor.

[0017] One object of the invention, among many, is to provide a monolithically-integrated dual surge protective device, which can enhance effect of surge prevention and can be integrated on a chip, and its fabrication method.

[0018] For an exemplary monolithically-integrated dual surge protective device, the detailed preferred embodiments include a LDMOS device and a diode assembly which comprises multiple diodes series-wound on back to back basis in the following sequence: -N-P- . . . -N-P-N-P-N- . . . -P-N-.

[0019] One end of the diode assembly is connected to the drain electrode of the LDMOS device and the other end is connected to gate electrode of the LDMOS device.

[0020] The diode assembly is fabricated and formed on thin film polysilicon by means of ion injection technique. More specifically, the diode assembly can be fabricated on gate oxide layer between the drain electrode and gate electrode of the LDMOS device.

[0021] The width-to-length ratio of channel of the LDMOS device is preferably 10 or more. For example, the length and width of the channel of the LDMOS device are 5 and 50 microns respectively.

[0022] In one example, an exemplary protective device can have multiple parallel connections.

[0023] For an exemplary fabrication method of an exemplary monolithically-integrated exemplary dual surge protective device, in one example, the diode assembly is fabricated in the gate electrode area of the LDMOS device after fabrication of the LDMOS device is completed, including the following steps in detail:

[0024] First, one polysilicon layer with thickness of 0.5 to 3 micron(s) is deposited on gate oxide layer of the LDMOS